UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/984,562	12/03/97	MAILLOUX J	95-0653.02

021186 LM02/1210
SCHWEGMAN LUNDBERG WOESSNER & KLUTH
P O BOX 2938
MINNEAPOLIS MN 55402

EXAMINER	
KIM,H	
ART UNIT	**PAPER NUMBER**
2751	12

DATE MAILED: 12/10/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/984,562	Mailloux et al
Examiner	**Group Art Unit**
H. Kim	2751

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 9/14/99.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 22-32 and 59-65 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 22-32 and 59-65 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____

☐ Interview Summary, PTO-413

☒ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

Detailed Action

1. Claims 22-32 and 59-65 are presented for examination. Claims 59-65 have been added by the amendment filed on 9/14/99. This office action is in response to the Amendment filed on 9/14/99.

2. The status of the related U.S. applications or patents should be updated and/or included as appropriate in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification, if any. (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.)

3. It is noted that this application appears to claim subject matter disclosed in the co-pending section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending applications to avoid possible double patenting.

Claim Objections

4. Claims 59-65 are objected to under 37 CFR 1.75(b) as not substantially differing from claims 22-32.

The claims as written do not appear to be substantially different or to provide substantially

different patent protection.

Applicants are required to 1) cancel the objected to claims,(2) amend the claims so that they are substantially different from any other claims, or (3) provide sufficient reasons why the claims as presently written are substantially different or provide substantially different patent protection.

As to claim 63, it appears that there is no support in the specification for "a first multiplexer" and "a second multiplexer".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 22-32 and 59-65 are rejected under 35 USC § 103(a) as being unpatentable over

Manning, U.S. Patent 5,610,864 in view of *Ryan*, U.S. Patent 5,966,724.

As to claim 22, *Manning* discloses a memory circuit, comprises control logic (Fig. 1 Ref. 38), selection and temporary storage circuit (Fig. 1 Ref. 18) for a first external address (col. 4 lines 16-18 or lines 22-24), and a multiplexer (Fig. 1 Ref. 18) and the control logic for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and an EDO mode of operation (col. 6 lines 14-26).

Although Manning discloses pipeline mode, Manning does not specifically disclose a mode control logic for selecting a burst or a pipeline mode of operation. However, it was well known in the memory art that the control signal for selecting between a burst (col. 4 lines 25-26) and a pipeline mode of operation (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of the control signal for switching between a burst and a pipeline mode of operation of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

As to claims 23 and 24, Ryan. further discloses external mode select signal for the burst mode or the pipeline mode and for determining the selected mode control signal and enable signal (col. 4 lines 20-27) .

As to claim 25, Manning. further discloses write enable and output enable (Fig. 2).

As to claim 26, Manning. further discloses a counter (Fig. 1 Ref. 26).

As to claim 27, Manning. further discloses the counter is used in the burst mode (col. 4 lines 47-49). Ryan. also further discloses the counter is used in the burst mode (col. 4 lines 25-27).

As to claim 28, *Ryan* further discloses a second external address (col. 4 lines 20-25).

As to claim 29, Ryan. further discloses EDO modes (col. 4 line 24).

As to claims 30 and 31, Manning further discloses CAS delay latency during a write and read cycle (col.7 lines 35-37). Ryan also discloses CAS delay latency during a write (col. 5 lines 14-16) and read cycle (col.3 lines 59+)

As to claim 32, Manning further discloses an asynchronously accessible memory array (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16).

As to claim 59, *Manning* discloses an asynchronous dynamic random access memory

circuit (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16), comprises control logic (Fig. 1 Ref. 38), selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24), and a multiplexer (Fig. 1 Ref. 18) and the control signal for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and an EDO mode of operation (col. 6 lines 14-26).

Although Manning discloses pipeline mode, Manning does not specifically disclose a mode control signal for selecting between a burst and a pipeline mode of operation. However, it was well known in the memory art that switching between a burst (col. 4 lines 25-26) and a pipeline mode of operation (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of the control signal for switching between a burst and a pipeline mode of operation of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

As to claim 60, *Manning and Ryan* disclose the invention as claimed in claim 22. *Ryan* further discloses control logic for providing an external mode control signal selecting an external address signal (col. 4 lines 25-26).

As to claim 61, *Manning and Ryan* disclose the invention as claimed in claim 22. *Ryan* further discloses control logic for providing an external mode control signal selecting an internal address signal (col. 4 lines 20-25).

As to claim 62, *Manning* discloses a memory circuit, comprises control logic (Fig. 1 Ref. 38), selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24), and a multiplexer (Fig. 1 Ref. 18) and the control logic for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and an EDO mode of operation (col. 6 lines 14-26).

Although Manning discloses pipeline mode, Manning does not specifically disclose a a mode control signal for switching between a burst and a pipeline mode of operation. However, it was well known in the memory art that control signal for switching between a burst (col. 4 lines 25-26) and a pipeline mode of operation (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of the control signal for switching between a burst and a pipeline mode of operation of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

As to claim 63, *Manning and Ryan* disclose the invention as claimed in claim 62. *Ryan* further discloses a first multiplexer (Fig. 1 Ref 18) and a second multiplexer (Fig. 1 ref. 26) for receiving the second external address (col. 4 lines 20-25).

Response to Amendment

6. Applicant's arguments with respect to claims 22-32 and 59-65 have been considered but are deemed to be moot in view of the new grounds of rejection.

Applicant's argument on page 4 middle that the reference does not disclose switching the memory circuit between a burst mode and a pipeline mode is not considered persuasive. Although *Manning* discloses option of switching between burstEDO and standard EDO modes of operation (col. 6 lines 17-40) and "other memory architecture applicable to the current invention includes a pipelined architecture" (col. 5 lines 43-45), Ryan discloses switching the memory circuit between a burst mode and a pipeline mode (col. 4 lines 20-27) for the purpose of high data throughput (abstract lines 8-9). Therefore, broadly written claims are disclose by the references cited.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. USP 5966724, 19991012, Synchronous memory device with dual page and burst mode operations, Ryan, Kevin J.

2. US 5752269, 19980512, Pipelined microprocessor that pipelines memory requests to an external memory, Divivier, Robert J. , et al..

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

9. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the Examiner

should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

13. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051-2, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Patent Examiner
November 23, 1999

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER